WHAT IS CLAIMED IS:

1. A data driver for a display device which has a clock input, a clock output, a plurality of data inputs and a plurality of data outputs, the data driver comprising:

an inverter chain including

a plurality of inverters which are serially connected to each other,

a first current source connected to a power supply side of any one of the plurality of inverters, and

a second current source connected to a ground side of any one of the plurality of inverters,

wherein a first stage inverter of the plurality of inverters receives the clock input, and an end stage inverter of the plurality of inverters supplies the clock output;

a smoothing circuit for smoothing the clock output to obtain an average voltage;

a comparator for comparing the average voltage with a reference voltage, wherein if the average voltage is lower than the reference voltage, the comparator supplies a first control voltage to control the magnitude of an electric current in the first current source such that the duty ratio of the clock output increases, and if the average voltage is higher than the reference voltage, the comparator outputs a second control voltage to control the magnitude of an electric current in the second current source such that the duty ratio of the clock output decreases; and

latching means for latching the plurality of data inputs in synchronization with the clock output and supplying results of the latches as the plurality of data outputs to a display section of the display device.

2. A data driver according to claim 1, wherein:

the inverter chain includes serially-connected first, second, third and fourth inverters; and

the first current source is connected to a power supply side of the first inverter, and the second current source is connected to a ground side of the third inverter.

3. A data driver according to claim 1, wherein:

the inverter chain includes serially-connected first and second inverters; and

the first current source is connected to a power supply side of the first inverter, and the second current source is connected to a ground side of the first inverter.

4. A data driver according to claim 1, further comprising a plurality of data inverter chains between the plurality of data inputs and the latching means,

wherein each of the plurality of data inverter chains has the same internal structure as that of the inverter chain that supplies the clock output, and

in each data inverter chain, an electric current control is performed based on the first and second control voltages.

5. A data driver according to claim 1, wherein:

the inverter chain further includes

a first auxiliary current source connected in parallel to the first current source, and

a second auxiliary current source connected in parallel to the second current source; and

the first and second auxiliary current sources are not controlled based on the

first or second control voltage.

6. A data driver according to claim 1, further comprising level shift means for increasing a small amplitude of each of the clock input and the plurality of data inputs to a predetermined level inside the data driver.

7. A data driver according to claim 1, further comprising a reference voltage generation circuit for supplying a variable reference voltage to the comparator.